APPENDIX A

1-20 (Cancelled).

21 (Currently Amended). A circuit comprising:

an output driver;

a data receiver;

a clock receiver ~~for receiving a~~ to receive at least one first clock signal having an embedded command and to output a second clock signal having the embedded command in response to receiving the first clock signal; and

a calibration path selectively configurable to couple an output of a selected one of the data receiver and the clock receiver to an input of the output driver based at least in part upon the embedded command of the clock signal.

22 (Cancelled). The circuit of claim 21, wherein the clock signal comprises an embedded command, wherein the calibration path is selectively configurable to couple one of the data receiver and the clock receiver to the output driver based at least in part upon the embedded command.

23 (Currently Amended). The circuit of claim ~~22~~21, further comprising:

a first multiplexer coupled to the data receiver and the clock receiver, the first multiplexer outputting ~~passing the~~ second clock signal received from ~~by~~ the clock receiver when a first multiplexer control signal is in a first logic state, and outputting ~~passing an input~~ a data signal received from ~~by~~ the data receiver when the first multiplexer control signal is in a second logic state.

24 (Currently Amended). The circuit of claim 23, further comprising:

a second multiplexer coupled to the first multiplexer and the output driver, the second multiplexer passing a signal output from the first multiplexer when a second multiplexer control signal is in a first logic state, and passing an output data signal when the second multiplexer control signal is in a second logic state~~, the signal output from the first multiplexer being the clock signal when the first multiplexer control signal is in the first logic state, and being the input data signal when the first multiplexer control signal is in the second logic state~~.

25 (Currently Amended). The circuit of claim 24, further comprising:

a serial-to-parallel shift register coupled to the data receiver, the second clock signal clocking the serial-to-parallel shift register.

26 (Currently Amended). The circuit of claim 25, further comprising:

a parallel-to-serial shift register coupled to the second multiplexer, the parallel-to-serial shift register providing the output data signal to the second multiplexer, the second clock signal clocking the parallel-to-serial shift register.

27 (Currently Amended). The circuit of claim 26, further comprising:

a logic circuit coupled to the first multiplexer[,] and the second multiplexer, ~~and the parallel-to-serial shift register,~~ the logic circuit receiving the second clock signal and setting the logic states of the first and second multiplexer control signals based at least in part upon the embedded command.

28 (Currently Amended). The circuit of claim 26, further comprising:

a logic circuit coupled to ~~the first multiplexer, the second multiplexer, and~~ the parallel-to-serial shift register,

the logic circuit receiving the second clock signal and ~~outputs~~ outputting a data pattern to the parallel-to-serial shift register based at least in part upon the embedded command.

29 (Currently Amended). The circuit of claim 26, further comprising:

an internal circuit coupled to the clock receiver, the serial-to-parallel shift register, and the parallel-to-serial shift register, the internal circuit receiving the second clock signal ~~received by~~ output from the clock receiver, receiving parallel input data from the serial-to-parallel shift register, and outputting parallel output data to the parallel-to-serial shift register.